Design of a Full Adder using PTL and GDI Technique

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Abstract: In this paper an area and power efficient 9T adder design has been presented by hybridizing PTL and GDI techniques. The proposed adder design consists of 5 NMOS and 4 PMOS transistors. A PTL based 5T XOR-XNOR module has been proposed to improve area at 130nm technology. The proposed Hybrid full adder design is based on this area efficient 5T XOR-XNOR module design. Different logic functions can be implemented by only two transistors by using Gate diffusion input (GDI) approach. To improve area and power efficiency a cascade implementation of XOR module has been avoided in the proposed full adder. XOR-XNOR modules outputs act as input to Carry and Sum module which has been implemented by the GDI MUX. GDI approach is suitable for design of high speed, power efficient circuits with improved logic level swing and static power characteristics using a reduced number of transistors as compared to CMOS techniques. Simulations have been performed using tanner tool and Result shows that the proposed adder has an improvement of 62% in power over Existing Parallel Self-timed Adder (PASTA).

Keywords: Recursive adder, CMOS design, Gate Diffusion Input, Pass transistor logic